Émeraude

Memristor-based Spiking Neural Network: Coding and Architecture

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Slide 1

1 Mahyar Shahsavari; 21-1-2014

Are We In The Appropriate Time For Neuro-inspired Computing?

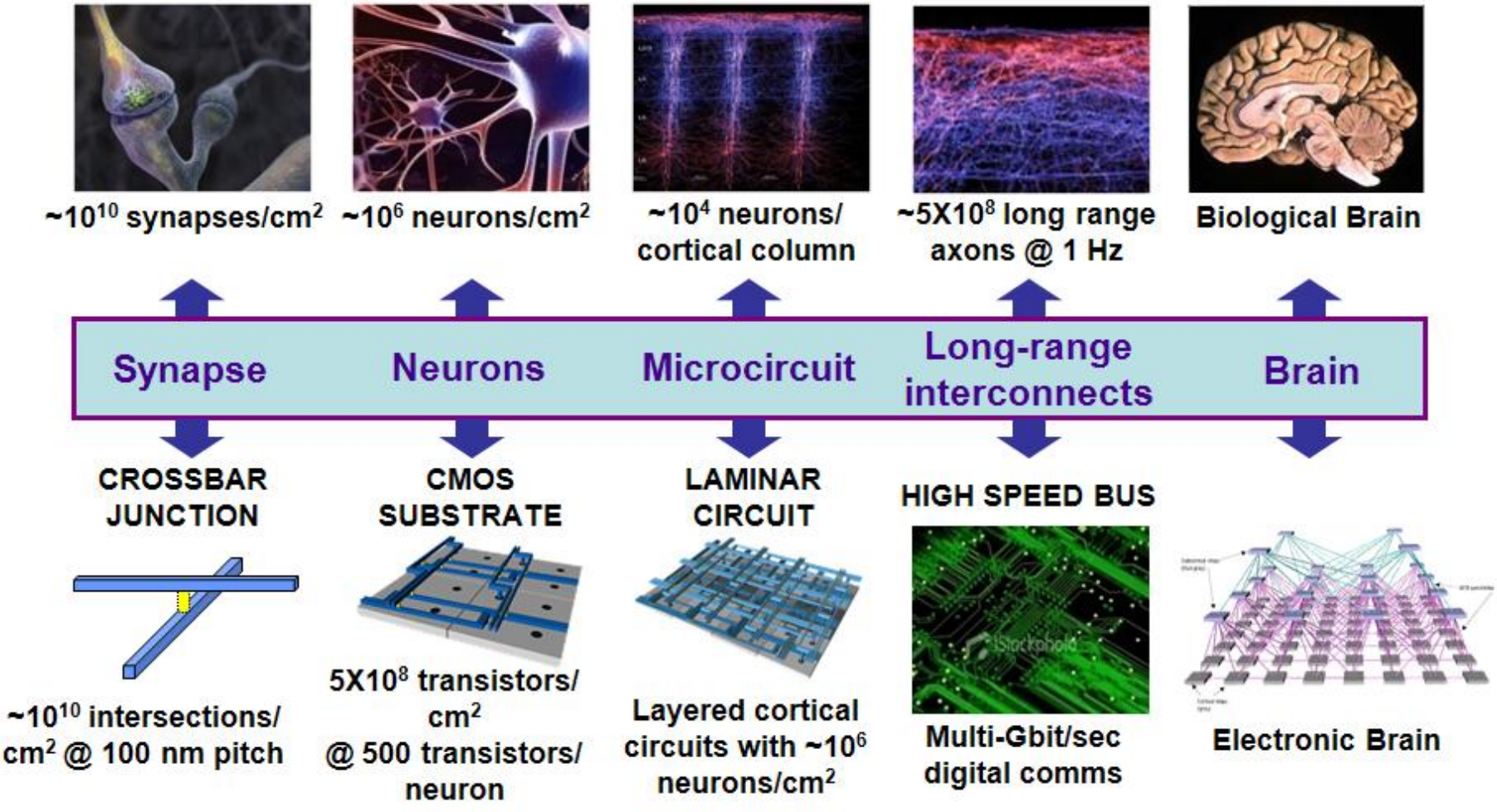
Sufficiently reliable non-volatile analog memory does not (yet) exist. (Murray-Elias, 1999)

- Consume much less power
- Take less area
- Easily Interfaced with the analog real world

However:

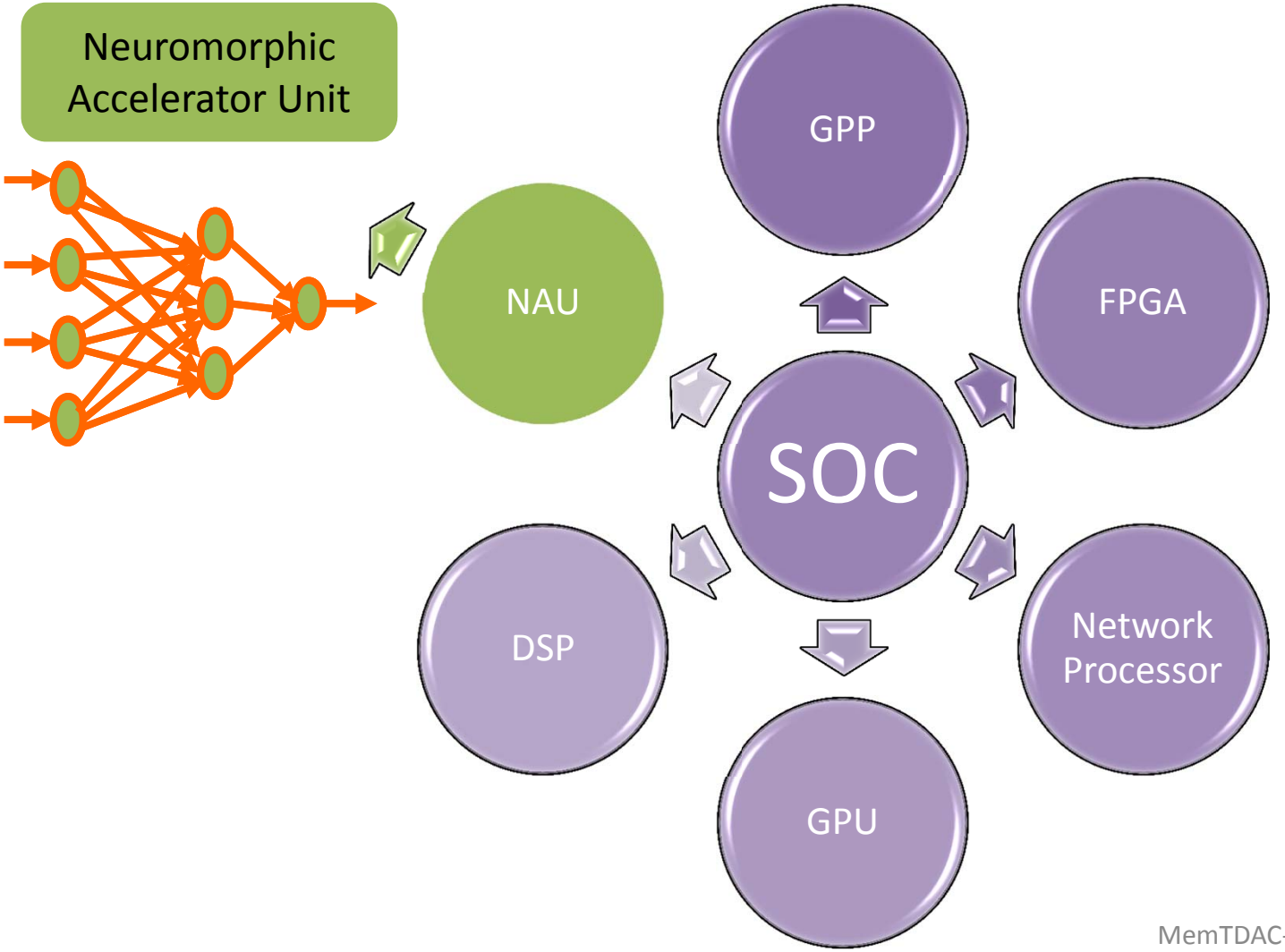
Analog Computation is inaccurate!

Are We In The Appropriate Time For Neuro-inspired Computing?

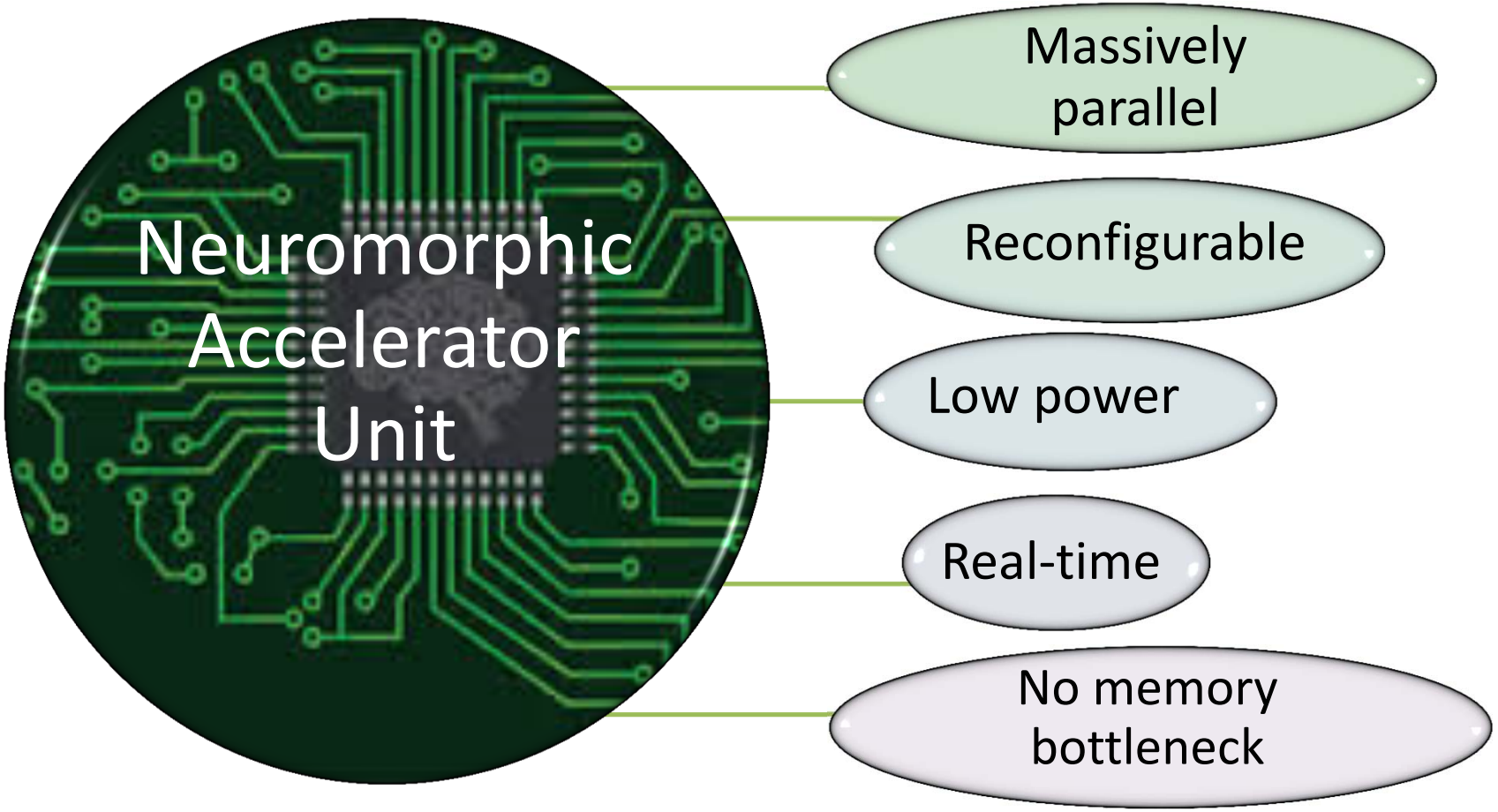


Reference : www.darpa.mil

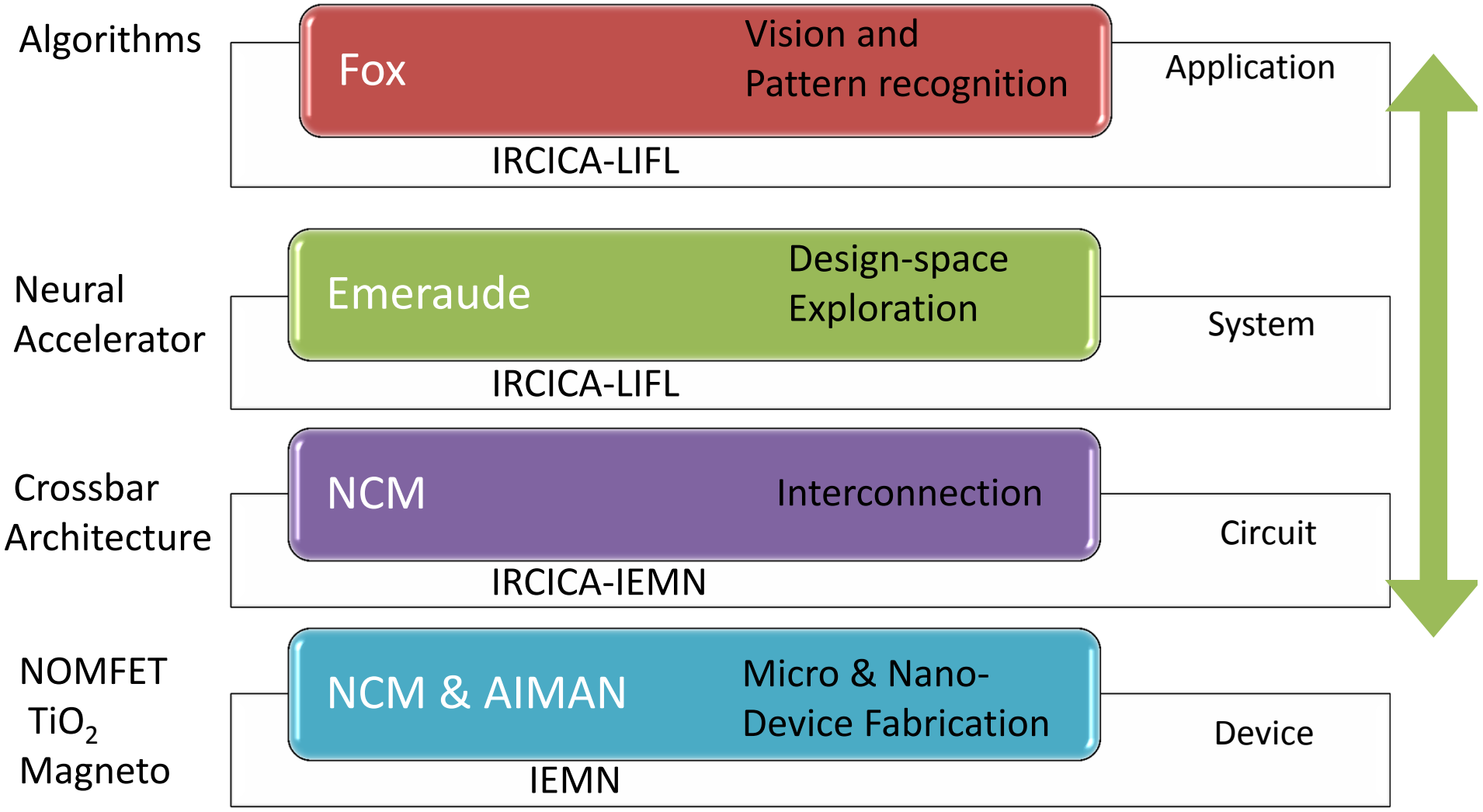
Neuromorphic Accelerator In Heterogeneous Platform



Accelerator Characteristics



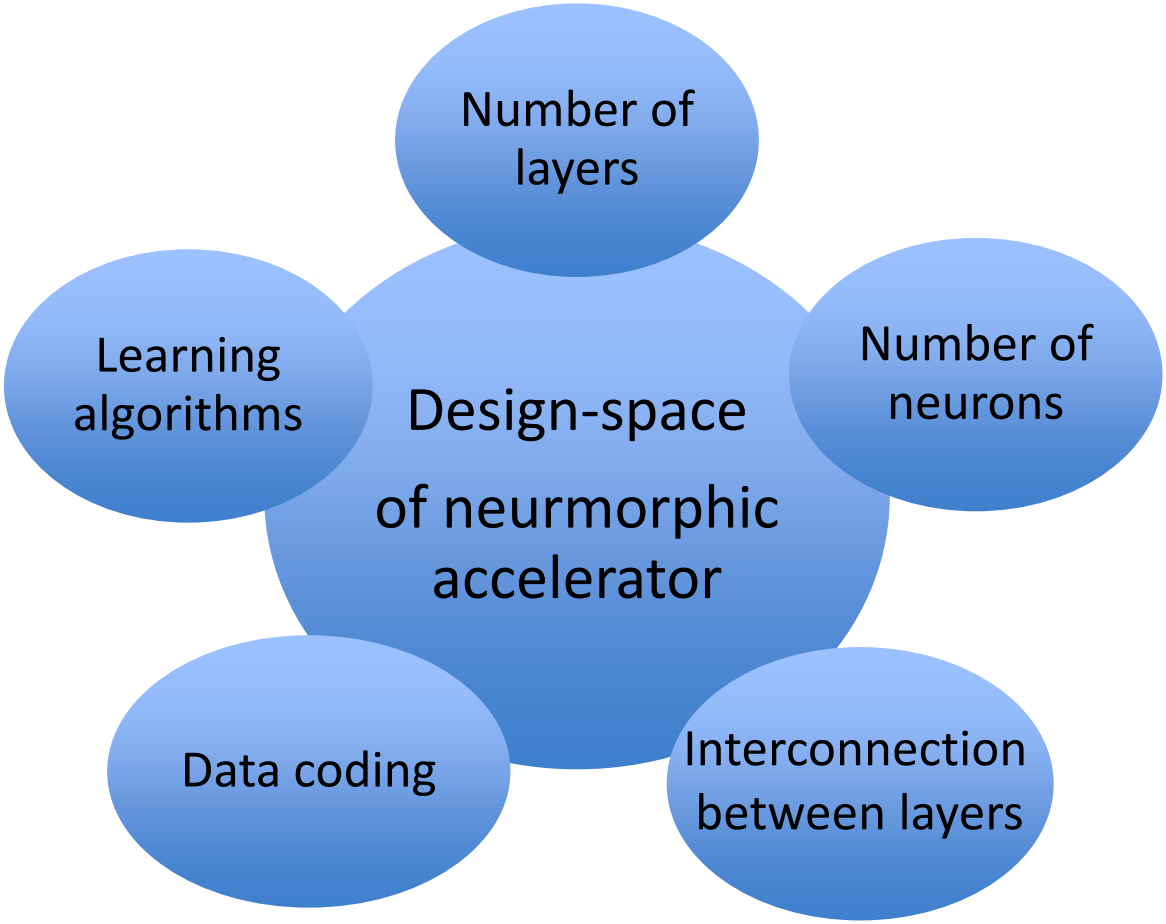
Interdisciplinary Project



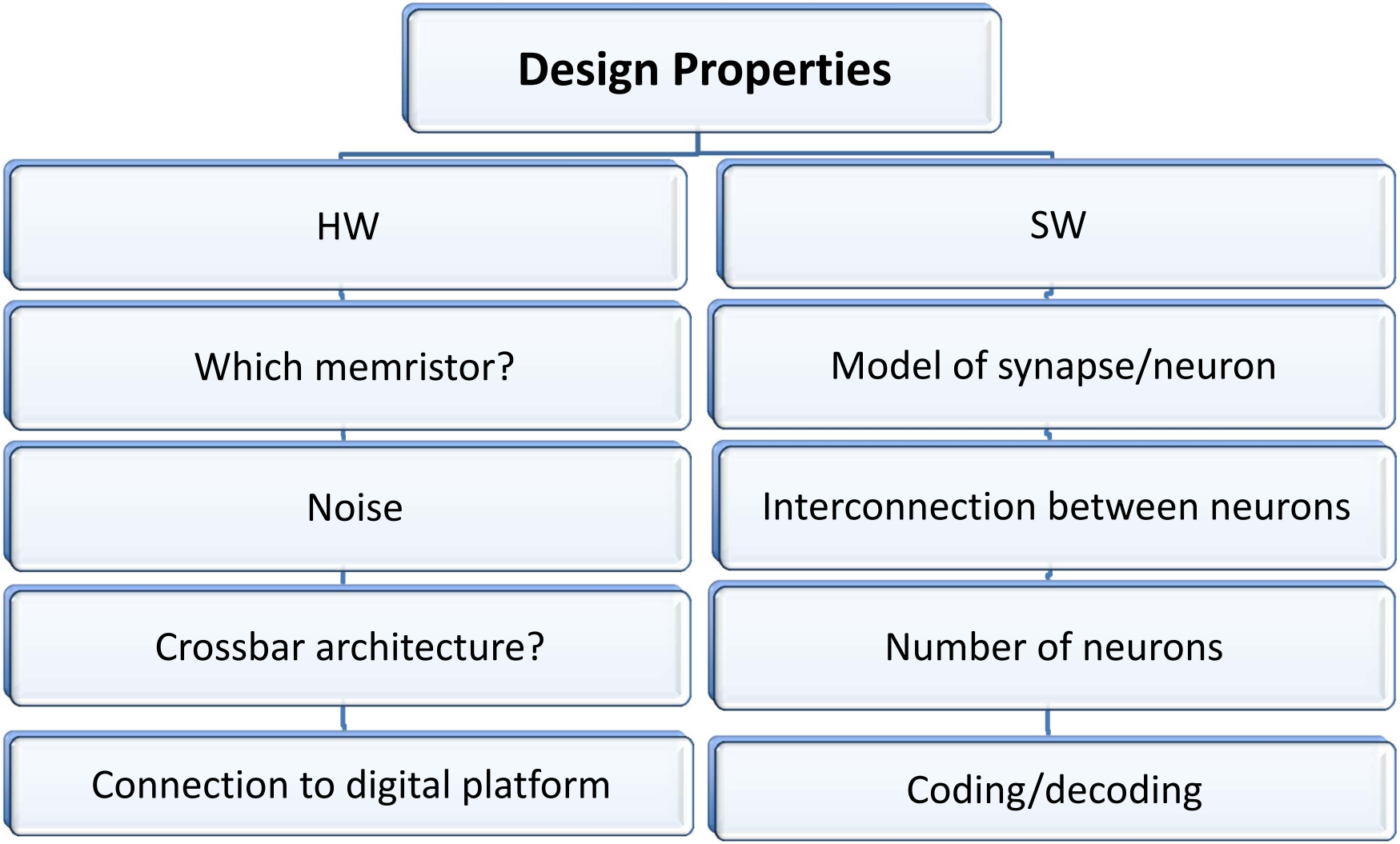
Interdisciplinary Project

- Testing different learning algorithms
- Neuro-inspired accelerator simulator
- Spike coding/decoding
- Designing crossbar array architecture
- Designing neuro-inspired accelerator hardware platform
- Fabrication different types of Memristor (TiO2, Organic, Magneto)

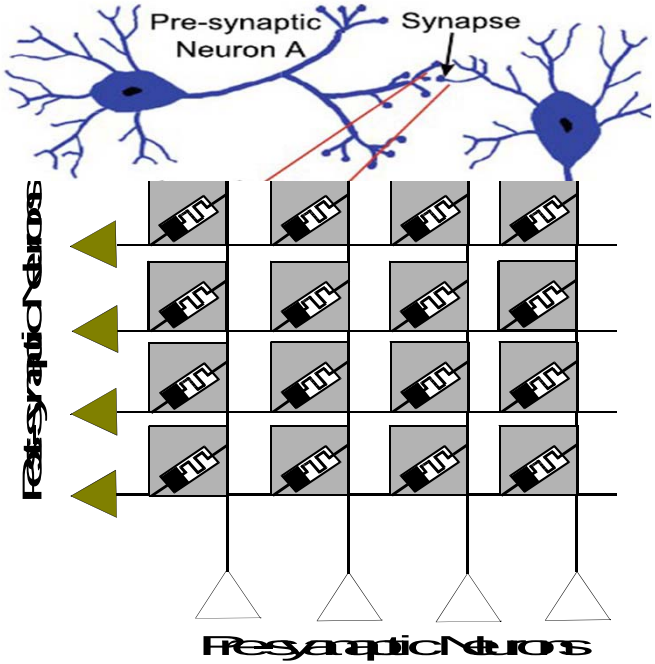
Design-Space Exploration (DSE)

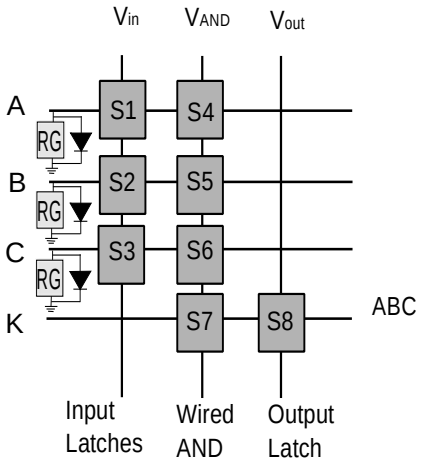


Design-Space Exploration (DSE)

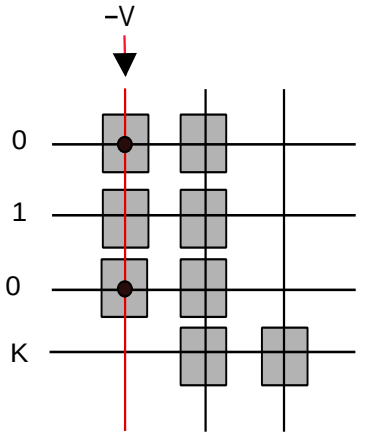


Crossbar architecture

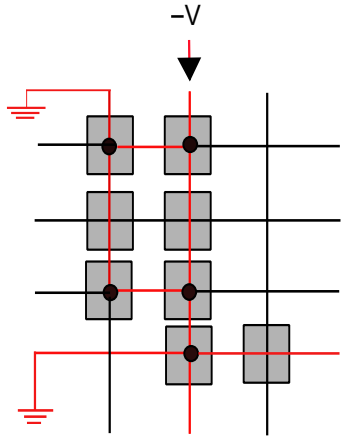




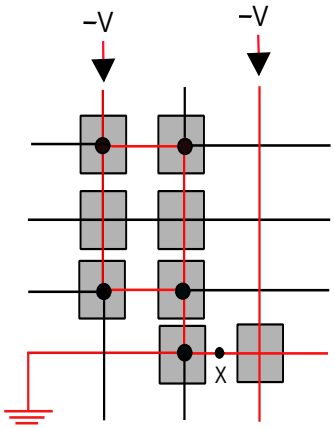
a: All latches opened



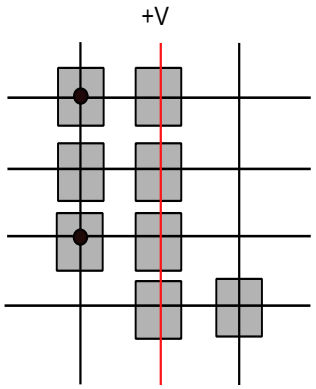
b: Input data latched



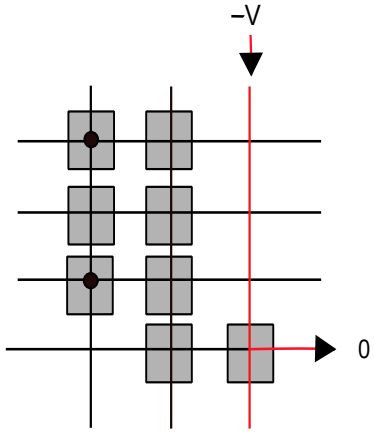
C: Wired-AND junctions closed



d: Wired-AND computed latched



e: Wired-AND junctions opened

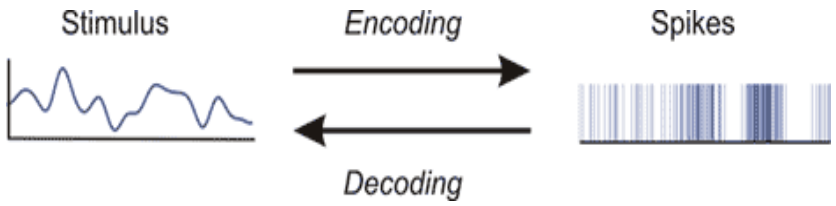


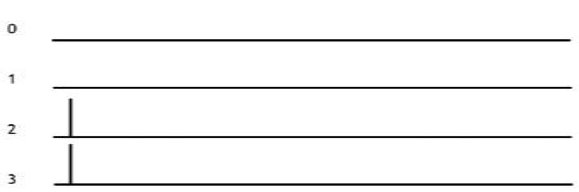
f: Read the output

Different Memristors

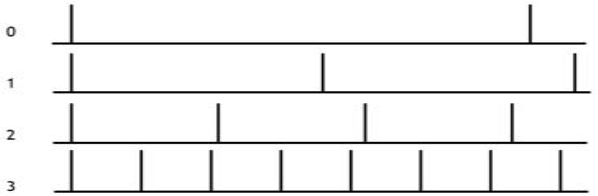
Memristora	Advantages	Disadvantages	Applications	University, Lab
Tio_2	Small scale, Fast switching, Simple structure	Still Non-reliable for commercial	Memory, Gate, analog, Neuromorphic	HP lab, IEMN,..
Spintronic	Magnetic Memory Match technology	Slow switching Non-CMOS compatible	RRAM, Sensing Scheme	University of pittsburgh, IEMN,..
Organic	Ultra-low power	Slow switching	Neuromorphic	Parma University, IEMN,…
Amorphous-si	CMOS compatible, Fast switching	Need high voltage forming process	Neuromorphic, Memory	Michigan University
Ferroelectric	For non-volatile memory array	Slow switching, Non-CMOS compatible	RRAM	Panasonic, Thales France

Information (Trans-)Coding





Threshold

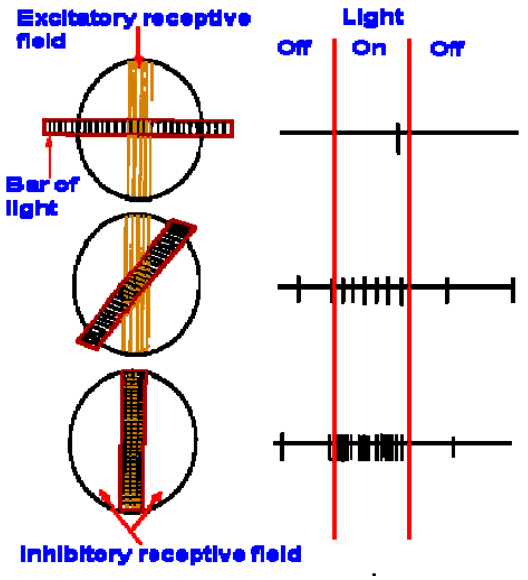


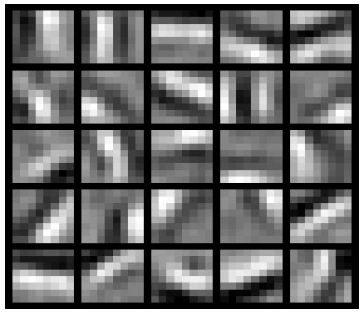
Rate

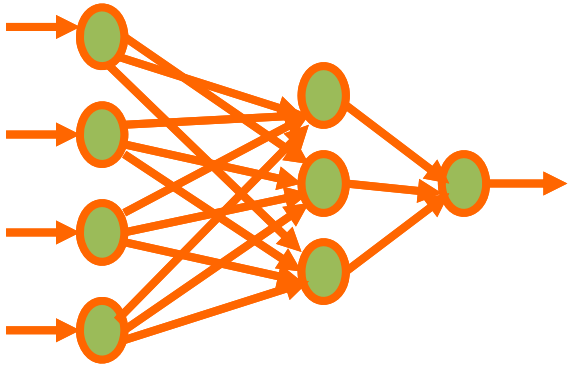
Spike-count

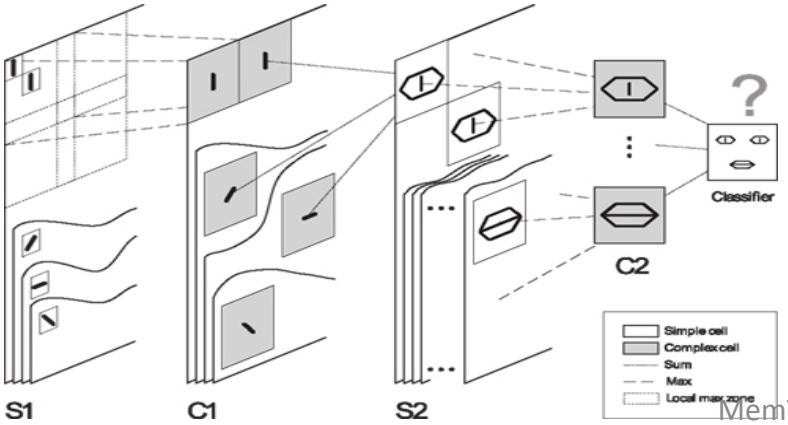
Temporal

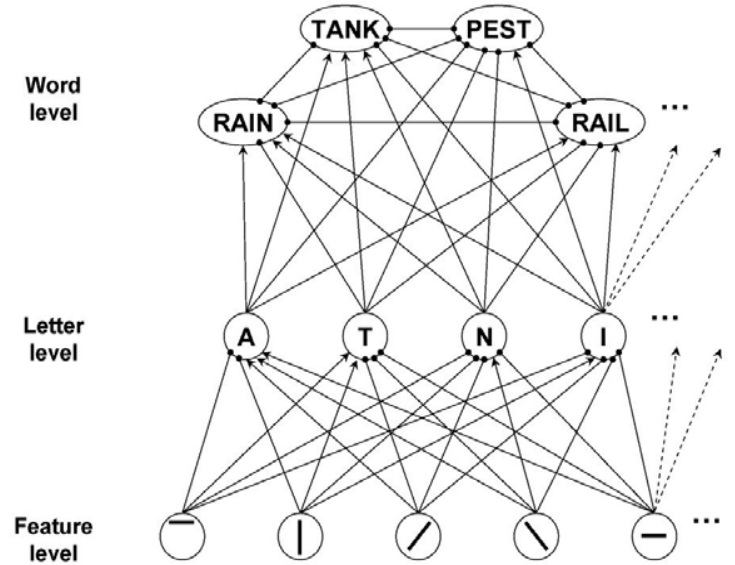
Unsupervised Learning











Simulators

- Brian: Brian is a simulator for spiking neural networks (python).
- Nest: Focus on the dynamics, size and structure of neural systems rather than on the exact morphology of individual neurons (python)
- CSIM: Tool for simulating heterogeneous networks composed of different model neurons and synapses(C++)
- Xnet: propose and validate an architecture based on nanoscale synapses that use both supervised and unsupervised (C++)
- Topographica, DANA,…

Suggestion!

Question?

Comments!

Contributions!